IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please amend the title as follows:

TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE ~~AND RESULTING STRUCTURE~~

IN THE SPECIFICATION:

Please amend the paragraph added by Examiner's Amendment as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a Divisional of U.S. ~~Application S.N.~~ Patent Application Serial No.~~08/789470, filed 01/27/1997,~~ 08/789,470, filed January 27, 1997, now U.S. Patent ~~6322634~~6,322,634, issued November 27, 2001.

Please amend the first full paragraph appearing on page 2 as follows:

Field of the Invention: The present invention relates to an apparatus and method for forming a shallow trench isolation structure. More particularly, the present invention relates to forming the shallow trench isolation structure using a buffer film layer etched such that a capped trench structure is formed ~~which~~ that isolates the shallow trench corners.

Please amend the third full paragraph appearing on page 3 as follows:

Numerous techniques have been proposed to overcome the ~~above discussed~~ above-discussed corner effects. ~~Commonly owned~~ Commonly owned U.S. Patent 5,433,794, issued July 18, 1995 to Fazan et al., hereby incorporated herein by reference, and U.S. Patent 5,521,422, issued May 28, 1996 to Mandelman et al., each teach forming shallow trench isolation structures wherein insulating material spacers are formed abutting the trench corners and the isolating material filling and extending above the trench. When a wet pad oxide etch is performed, the isolating material combines with the spacers to form an isolation trench having a ~~dome~~ dome- or cap-like covering the peripheral edges of the ~~trench~~ trench, which substantially overcomes the corner effects and consequential leakage between active areas on the substrate. Although the techniques taught in these patents are effective in minimizing corner effects, the techniques require additional fabrication ~~steps~~ steps, which increase the overall cost of the semiconductor component.

Please amend the first full paragraph appearing on page 4 as follows:

Therefore, it would be advantageous to develop a shallow isolation trench and a technique for forming the trench ~~which~~ that substantially eliminates the aforementioned corner effects, while using inexpensive, ~~commercially available, widely practiced~~ commercially available, widely practiced semiconductor device fabrication techniques and apparatus.

Please amend the second full paragraph appearing on page 4 as follows:

The present invention relates to a shallow isolation trench structure ~~which~~ that is formed using a buffer film layer. The buffer film layer is etched in such a manner that an isolation material within the shallow trench has a cap ~~which~~ that covers the shallow trench corners to prevent corner effects.

Please amend the third full paragraph appearing on page 4 as follows:

The method of the present invention comprises providing a semiconductor substrate, preferably a silicon substrate, with a dielectric layer, preferably silicon dioxide, formed on at least one surface of the semiconductor substrate to a thickness of ~~between 50~~ between 50Å and 300Å. The dielectric layer can be formed by any known technique, including thermally oxidizing the surface of the semiconductor substrate, chemical vapor deposition, sputtering, or the like. A buffer film layer, preferably silicon nitride, is then formed over the dielectric layer by any known deposition technique, preferably chemical vapor deposition. Although silicon nitride is preferred, the buffer layer may be any known material ~~which~~ that is oxidation resistant and can be etched selectively to oxide films.

Please amend the fourth full paragraph appearing on page 4 as follows:

A photoresist mask is applied and patterned on the buffer film layer. The buffer film layer, the dielectric layer, and semiconductor substrate are then etched either simultaneously with a non-selective etch or in steps with selective etches to form a shallow trench with ~~sidewalls~~ side walls and a bottom. The photoresist mask is then removed to form a trenched structure.

Please amend the first full paragraph appearing on page 5 as follows:

After stripping the photoresist and cleaning the trenched structure, a thin layer of oxide, between ~~about 50~~ about 50Å and 150Å thick, is grown on the shallow trench ~~sidewalls~~ side walls and bottom, preferably by thermal oxidization. The buffer film layer is then selectively etched horizontally and vertically to move the buffer film layer back from the shallow trench. The purpose for using a buffer film layer, which is oxidation resistant, as discussed above, is shown in FIG. 11. If an oxidizable material is used as a buffer film layer 202 over a dielectric layer 204 and a substrate 206, the formation of a thin oxide layer 208 in trench 210 would also cause the formation of an additional thin layer of oxide 212 to form on the buffer film layer 202. Most oxidizable materials, such as silicon dioxide, used for forming the buffer film layer 202 have a greater affinity for growing oxides than the semiconductor substrate. As a result, the additional thin oxide layer 212 is relatively thicker than the thin oxide layer 208, which results in a narrowing of the opening at the mouth of the trench 210. This narrowing makes it difficult to fill the trench 210 with an isolation material 214, and may even cause the formation of voids 216 in the isolation material 214 during the application of the isolation material 214.

Please amend the paragraph bridging pages 5 and 6 as follows:

In the method of the present invention, after etching back the buffer film layer, the shallow trench is then filled with an isolation material. The resulting structure is preferably annealed to densify the deposited isolation material. Densification of the deposited isolation material is required to enhance the resistance of the isolation material to etching during subsequent processing. A portion of the isolation material over the buffer film layer is then removed to the level of the buffer film layer. The removal of isolation material is preferably achieved with a process such as ~~chemical mechanical~~ chemical-mechanical planarization ~~which~~ that abrades away the isolation material down to the buffer film layer. The buffer film layer is then selectively ~~etch~~ etched away to form an isolation structure. When this isolation structure is etched during a subsequent wet oxide etch process, the isolation structure will form the capped shallow trench isolation structure ~~which~~ that covers the trench corners. This capped shallow trench isolation structure substantially minimizes corner effects.

Please amend the fourth paragraph appearing on page 6 as follows:

FIGS. 1 through 10 illustrate, in cross-section, a method for forming a shallow trench isolation structure in accordance with one embodiment of the present invention. As shown in FIG. 1, the method comprises forming a layered structure 100 of a semiconductor substrate 102, a dielectric layer 104, and a buffer film layer 106. The semiconductor substrate 102 preferably includes silicon and the dielectric layer 104 preferably includes silicon dioxide. The dielectric layer 104 is preferably ~~between 50~~ between 50Å and 300Å thick (a convenient range for process integration) and can be formed by any known technique including thermally oxidizing the surface of the semiconductor substrate 102, chemical vapor deposition, sputtering, or the like. The buffer film layer 106, preferably comprising silicon nitride, is formed over the dielectric layer 104 by any known deposition technique, preferably chemical vapor deposition.

Please amend the paragraph bridging pages 6 and 7 as follows:

A photoresist mask 108, either a positive or negative resist (preferably positive) as known in the art, is applied over the buffer film layer 106 and patterned using standard photolithographic patterning techniques, as shown in FIG. 2. The buffer film layer 106 and the dielectric layer 104 are then etched by standard etching techniques to form patterned recess 110, as shown in FIG. 3. The silicon substrate 102 is then dry etched to form a shallow trench 112 with ~~sidewalls~~ side walls 114 and a bottom 116, seen in FIG. 4. It is, of course, understood that the buffer film layer 106, the dielectric layer 104, and semiconductor substrate 102 can be etched in one non-selective etching step. The photoresist mask 108 is removed using standard photoresist stripping techniques, preferably by plasma etch, to form a trenched structure 118, as shown in FIG. 4.

Please amend the first full paragraph appearing on page 7 as follows:

After stripping the photoresist and cleaning (preferably with an H_2O_2/H_2SO_4 or H_2O_2/HCl mixture) the trenched structure 118, a thin layer of oxide 120, between ~~about 50~~ about 50Å and 150Å thick, is grown on the shallow trench ~~sidewalls~~ side walls 114 and the shallow trench bottom 116, preferably by thermal oxidization, as shown in FIG. 5. As shown in FIG. 6, the buffer film layer 106 is then selectively etched horizontally and vertically to move the buffer film layer 106 back from the shallow trench 112. The etching of the buffer film layer 106 is preferably a wet etch process including an application of a 100:1 HF (hydrofluoric acid) solution followed by an application of a H_3PO_4 (phosphoric acid) solution or an ~~H2O~~ $H_2O/N(CH_2CH_3)_4OH$ ~~("TMAH")~~ (TMAH) solution.

Please amend the paragraph bridging pages 7 and 8 as follows:

As shown in FIG. 8, the isolation material 122 is removed down to the buffer film layer 106, preferably by a mechanical abrasion process, such as ~~chemical/mechanical~~ chemical-mechanical planarization. The buffer film layer 106 is then selectively etched ~~away,~~ away by any known ~~technique~~ technique, such as a hot H_3PO_4 (phosphoric acid), to form an isolation structure 124, as shown in FIG. 9. When this isolation structure 124 is etched during a subsequent wet oxide process to expose ~~the upper~~ an upper surface 132 of said semiconductor substrate 102, the isolation structure 124 will form a capped shallow trench isolation structure ~~126~~ 126, which covers ~~the trench~~ trench corners 128 of the shallow trench 112 with ledges 130, as shown in FIG. 10. The ledges 130 preferably extend horizontally between ~~about 50~~ about 50Å and 150Å from the trench corners 128. These ledges 130 prevent the aforementioned corner effects.